WHAT IS CLAIMED IS:

1. A printhead circuit for correcting bow in a linear arrangement of elements comprising:

a substrate assembly for an image exposure line arrangement of a printer, a plurality of LED elements representing said image exposure line arrangement, each LED element having an associated driver subassembly on said substrate assembly and, each of said LED elements representing a pixel within an image exposure line;

an interface board coupled to said substrate assembly, said interface board having circuitry that processes image exposure data for said LED elements;

a course bow correction circuit on said interface board that electronically arranges the pixels generated by said LEDs to improve linearity by integral numbers of pixel pitches; and

a fine bow correction circuit located at least partially on said substrate assembly, said fine bow correction circuit providing a first circuit common to a plurality of said LED elements and a second circuit dedicated to a specific LED element, said second circuit selecting one of a set of delays in activating said LED such that linearity of the pixels within an image exposure line is improved by a fraction of a pixel pitch.

3. The printhead circuit of claim 1, wherein said fine bow correction circuit is located at least partially on said interface board.

4. The printhead circuit of claim 3, wherein said fine bow correction circuit that is located at least partially on said interface board provides at least one circuit trace that carries a plurality of signals to said fine bow correction circuit on said substrate assembly, wherein the signals are not concurrently active.

5. The printhead circuit of claim 1, wherein with said fine bow correction, said first circuit provides said set of delays for said plurality of LED elements; and

said second circuit selects one of the delays from said set of delays according to a specific parameter for said specific LED element.

6. The printhead circuit of claim 5, wherein said parameter further comprises a stored value that enables said second circuit to select one of the delays from said set of delays.

7. The printhead circuit of claim 6, wherein said stored value is within said fine bow correction circuit, and said fine bow correction circuit further comprises at least one multiplexer and at least one latch per LED element.

8. The printhead circuit of claim 1, further comprising a delay repeat circuit that creates multiples of said set of delays using said set of delays.

9. The printhead circuit of claim 1, wherein said fine bow correction circuit is implemented at a segment level selected from one of the following LED segment level groupings: 2, 4, 8, or 16 LED elements.

10. The printhead circuit of claim 1, wherein said interface board further comprises a set of printhead brightness tables and a set of printhead correction tables on said interface board.

11. The printhead circuit of claim 1, wherein said LED elements are arranged in a plurality of rows and wherein said second circuit selects different delays, from said set of delays, for different rows of LED elements.

12. The printhead of claim 11, wherein said plurality of rows of LED elements further comprises an odd row and an even row, and said second circuit selects delays that are offset by a period substantially equal to a selected delay, between an odd row and an even.

22. A method for producing an electronic printhead, having pixel alignment circuitry, by the steps of:

providing a substrate having a plurality of printing elements representing an image exposure line, with associated driver circuitry, coupled to an interface board, and timing means for selectively activating said printing elements for exposing an image exposure line, one at a time, for a preselected exposure period, each of said printing elements representing a pixel within an image exposure line;

creating a coarse adjustment circuit on said interface board, said coarse adjustment circuit having circuitry that aligns image exposure line pixel data in integral numbers of lines;

forming a fine adjustment circuit located at least partially on said substrate, said fine adjustment circuit providing a plurality of delays to each of said printing elements, wherein each of said delays is a fraction of an exposure period of said timing means corresponding to a fraction of a pixel pitch; and

selecting one of the delays in accordance with a predetermined parameter.

23. The method of claim 22, wherein said step of forming further comprises forming said fine adjustment circuit with a software accessible register for delay selection of each printing element.

24. The method of claim 22, wherein said step of forming further comprises forming a fine adjustment circuit wherein a software accessible register can be loaded via a JTAG serial data path.

25. The method of claim 24, wherein the step of forming further comprises forming the fine adjustment circuit wherein a delay clock having a fixed clock reference for unique fixed delays has a frequency that can be changed to produce different delay increments.

26. The method of claim 22, wherein said step of forming further comprises forming a fine adjustment circuit wherein a plurality of delays are modifiable to allow for different levels of pixel fine adjustment.

27. The method of claim 22, wherein said step of forming said fine adjustment circuit, forms a fine bow correction circuit located at least partially on said interface board, and provides at least one circuit trace that carries a plurality of signals to said fine bow correction circuit on said substrate, wherein said signals are not concurrently active.

28. The method of claim 22, wherein said step of selecting further comprises selecting said delays such that said delays are repeated with a first delay following a last delay forming a repeated delay circuit from multiples of said delays.

29. (Currently Amended) The method of claim 22, wherein said step of providing further comprises providing said printing elements arranged in a plurality of rows, and wherein said fine adjustment circuit selects different delays for different rows of said printing elements.

30. The method of claim 29, wherein said step of providing further comprises providing as said plurality of rows, an odd row and an even row, and said fine adjustment circuit selects delays that are offset by one delay period between an odd row and an even row.